BSTZ No. 042390.P10353
Express Mail No. EL635877925US

UNITED STATES PATENT APPLICATION

FOR

~~OBSERVABILITY BUFFER~~

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FIELD

This invention relates to an observability buffer, more particularly, a buffer for unintrusively observing, and echoing to a diagnostic device, signals transmitted by one of a bus and wireless communication, without disturbing electrical properties of the bus, without adding bus latency, and without adding signal discontinuities.

BACKGROUND

Computer systems commonly use busses to transfer data between devices that include processors, storage devices and input/output (I/O) devices. Many of such busses use one or more data lines, which are electrical conductors on which signals are used to transfer data in concert with a clock signal and/or one or more control signals. In a ternary bus, each device must use the data it is transmitting to derive the data being received, and debugging such a bus to diagnose problems or confirm functionality is rendered more difficult. Diagnostic tools, such as a logic analyzer, have failed to monitor the data being transferred between two devices by the simple attachment of probes to the conductors of a ternary bus. Further, as computer systems move towards the use of multi-stage pipelines and large symmetric multiprocessor (SMP) shared cache structures, the ability to debug, analyze, and verify actual hardware becomes increasingly difficult, during development, testing, and normal operations.

BRIEF DESCRIPTION OF THE DRAWINGS

Additional advantages of the invention will become apparent upon reading the following detailed description and upon reference to the drawings, in which:

Fig. 1 depicts a schematic diagram of an embodiment of the invention;

Fig. 2 depicts a schematic diagram of an embodiment of the invention integrated on a component connected to a bus; and

Fig. 3 depicts a schematic diagram of an embodiment of the invention as in Fig. 2, the component being dynamic random access memory (DRAM).

DETAILED DESCRIPTION

Exemplary embodiments are described with reference to specific configurations. Those skilled in the art will appreciate that various changes and modifications can be made while remaining within the scope of the claims.

An increasing number of busses now transfer data at rates high enough that the attachment of probes to conductors of a bus will alter the electrical and/or timing characteristics of the bus such that data integrity is adversely effected or the functionality of the bus is impaired. It is often desirable for testing to monitor complex events so that useful debug and performance information can be captured in a fast, unintrusive manner. Further, efforts are currently being made to accelerate the convergence of voice, video and data in corporate networks and enable users to easily exchange larger graphics and imaging files. In an embodiment, the invention is used in high-speed network connectivity having data rates in the gigabit per second range.

In an embodiment, the invention provides an apparatus method and means for unintrusively observing, echoing and reading signals transmitted by one of a bus and wireless communication, without disturbing electrical properties of the bus, without adding bus latency, and without adding signal discontinuities.

In an embodiment, the invention provides an apparatus method and means to observe and echo bus signals for diagnostic purposes and other purposes. In an embodiment, the invention eliminates the need to directly probe a bus, and opens a way to use any form of signaling on a bus. A bus may be a simultaneous bi-directional (SBD) bus having ternary logic levels, not unintrusively observable by conventional bus probing techniques. In an embodiment, the present invention provides observability of signals on a SBD bus using conventional logic analysis techniques, while the bus operates at maximum speed.

In an embodiment, a buffer is provided that connects to a bus and observes and echoes signals transmitted on a bus. In an embodiment, the buffer is integrated on a component which connects to a bus. In an embodiment, the buffer echoes bus signals having frequencies between 500MHz. and 5GHz. In an embodiment, the buffer echoes bus signals having frequencies of at least 5 GHz.

An embodiment of the invention is shown as component 23 in **Fig. 1**. Buffer 9 and buffer 13, connected with bus 3a and bus 3d, observe signals transmitted on bus 3a and bus 3d. In an embodiment, bus 3a and bus 3d are SBD busses. In an embodiment, buffer 9 and buffer 13 observe and echo signals transmitted by wireless communication. In an embodiment, buffer 9 and buffer 13 are integrated on a component which connects to a bus. The signals from buffer 9 are echoed to observability port 5, and the signals from buffer 13 are echoed to observability port 7. In an embodiment, a diagnostic device, connected with observability bus 15 which is connected with observability port 5, performs at least one of detecting echoed signals, accessing echoed signals and reading echoed signals. Also, the diagnostic device, connected with observability bus 17 which is connected with observability port 7, performs at least one of detecting echoed signals, accessing echoed signals and reading echoed signals. In an embodiment, observability ports 5 and 7 are logic observability ports.

In an embodiment, bus 3a and bus 3d are memory busses. In an embodiment, bus 3a and bus 3d are one of data busses, address busses, and control busses. In an embodiment, buses 3a and 3d are one of a SBD bus having ternary logic levels, a single ended bus, a differential bus, a peripheral component interconnect (PCI) bus, an industry standard architecture (ISA) expansion bus, a chipset bus, a frontside bus, an I/O bus, and a bus over which a plurality of data are transmitted. In an embodiment, bus 3a and bus 3d are one of 16 bit busses, 32 bit busses, etc.

Although the present invention is described in the context of busses carrying signals across rigid interconnections spanning relatively short distances between electronic components within a computer system, in an

embodiment, the present invention is also applicable to the transmission of signals across cables or other flexible interconnections, including optical fibers, spanning longer distances between electronic components of computers or other varieties of electronic devices.

In an embodiment, bus 3a and bus 3d are ternary logic busses that enables the substantially SBD transfer of data in such a way that it is not possible for a third device to derive the data being transferred by attaching probes to conductors of bus 3a or bus 3d and monitoring the voltage levels of those conductors. In an embodiment, bus 3a and bus 3d transfers data at speeds sufficiently high, or rely on differences between voltage levels that are sufficiently small, that it is not possible to attach probes to the conductors of either bus 3a or bus 3d without altering the electrical characteristics of those conductors such that data integrity is adversely effected, or such that timing parameters required for normal operation of the bus are violated. In an embodiment, bus 3a and bus 3d are ternary logic busses enabling substantially SBD transfers at speeds sufficiently high that both difficulties are encountered when attaching probes to the conductors of bus 3a and bus 3d.

In an embodiment, buffer 9 and buffer 13 include at least one trigger to observe or capture signals. In an embodiment, the trigger operates in various manners. In one embodiment, buffer 9 and buffer 13 are expandable and capture every bus signal in a first in-first out basis. In an embodiment, a trigger instructs buffer 9 and buffer 13 to capture the following finite specific bus signals. In a further embodiment, a trigger provides a specific control signal and address signal instructing buffer 9 and buffer 13 to capture bus signals. In yet a further embodiment, buffer 9 and buffer 13 are triggered to capture bus signals at an indicated time.

As shown in **Fig. 2**, in an embodiment of the invention, buffer 4, buffer 6, buffer 8 and buffer 10 are integrated on component 76. Component 76 connects to a bus. In an embodiment, component 76 is a memory component. Buffer 4 observes signals on bus 12b, coming from I/O receiver 14, and continuing on to the core or array of component 76. Buffer 6 observes signals on bus 12c, coming from the core or array of component 76, and continuing on

to I/O transmitter16. Likewise, buffer 8 observes signals on bus 12d, coming from I/O receiver 18, and continuing on to the core or array of component 76. Buffer 10 observes signals on bus 12e, coming from the core or array of component 76, and continuing on to I/O transmitter 20. The signals from buffer 4 are echoed to observability port 50, the signals from buffer 6 are echoed to observability port 52, the signals from buffer 8 are echoed to observability port 56, and the signals from buffer 10 are echoed to observability port 54.

In an embodiment, diagnostic device 82, connected with observability bus 60 which is connected with observability port 50, performs at least one of detecting echoed signals, accessing echoed signals and reading echoed signals. Diagnostic device 82, connected with observability bus 62 which is connected with observability port 52, performs at least one of detecting echoed signals, accessing echoed signals and reading echoed signals. Diagnostic device 82, connected with observability bus 64 which is connected with observability port 54, performs at least one of detecting echoed signals, accessing echoed signals and reading echoed signals. Also, diagnostic device 82, connected with observability bus 66 which is connected with observability port 56, performs at least one of detecting echoed signals, accessing echoed signals and reading echoed signals. In an embodiment, diagnostic device 82 is one of a logic analyzer and a bus analyzer of the variety commonly used in debugging busses, however, diagnostics device 82 could be any of a variety of devices using signal inputs to aid in debugging busses. Although **Fig. 2** depicts the use of four ports and four busses in connecting component 76 and diagnostics device 82, the quantity and nature of the coupling is not so limited.

In an embodiment of the invention, as shown in **Fig. 3**, buffer 4, buffer 6, buffer 8 and buffer 10 are integrated on component 76 which connects to a bus. In an embodiment, component 76 is dynamic random access memory (DRAM). Components 72, component 74, and component 78 are also DRAM components which are connected with device 70 and device 80. In an embodiment, device 70 and device 80 are each one of a processor, a storage device, a graphics controller coupled to a display, an I/O device such as disk controller or an I/O interface for such devices as a keyboard, mouse or printer,

etc. Alternatively, in an embodiment, device 70 and device 80 are each a bridge device providing access to another bus.

In an embodiment, the invention can be used in components that connect to a memory bus, including DRAMs, chip sets, memory controllers, microprocessors, microcontrollers, etc.

In an embodiment, a system is provided. The system includes memory, an I/O port, and a microprocessor. The memory, I/O port, and microprocessor are connected by a data bus, address bus and control bus. The microprocessor includes a buffer having at least one trigger, coupled with one of the busses and a component connected with the busses, configured to observe and echo at least one of signals transmitted on the bus, signals transmitted into the component and signals transmitted out of the component. In an embodiment, the system includes an observability port coupled with the buffer configured to receive the echoed signals, an observability bus connected with the observability port, and a diagnostic device being at least one of a logic analyzer and a bus analyzer connected with the observability bus and performing at least one of detecting the echoed signals, accessing the echoed signals and reading the echoed signals. In an embodiment, the observability port is a logic observability port. In an embodiment, the bus is one of a SBD having ternary logic levels, a single ended bus, a differential bus, an optically coupled bus, a chipset bus, a frontside bus, an I/O bus, a PCI bus, and an ISA expansion bus. In an embodiment, the buffer is configured to observe and echo signals transmitted by wireless communication.

In an embodiment, a system is provided. The system includes memory, an I/O port , and a microprocessor. The memory, I/O port, and microprocessor are connected by a data bus, address bus and control bus. The microprocessor includes an apparatus having a means for observing and echoing at least one of signals transmitted on a bus, signals transmitted into a component and signals transmitted out of a component. In an embodiment, the apparatus includes means for receiving echoed signals, and means for performing at least one of detecting echoed signals, accessing echoed signals and reading echoed signals. In an embodiment, the bus is one of a SBD

having ternary logic levels, a single ended bus, a differential bus, an optically coupled bus, a chipset bus, a frontside bus, an I/O bus, a PCI bus, and an ISA expansion bus. In an embodiment, the signals are transmitted by wireless communication.

Having disclosed exemplary embodiments, modifications and variations may be made to the disclosed embodiments while remaining within the spirit and scope of the invention as defined by the appended claims.